

AMENDMENTS TO THE DRAWINGS

The attached replacement sheets of drawings include the Examiner's requested changes.

Attachment: Replacement sheets

REMARKS

Reconsideration and withdrawal of the rejections set forth in the Office Action dated March 24, 2005 are respectfully requested. In the Office Action, Claims 1, 5, 9, 13 and 14 stand rejected under 35 USC 102 (b) as being anticipated by Chang et al. (U. S. Patent No. 5,969,383). Claims 2, 3, 6, 7, 10, 11 and 15-21 stand rejected under 35 USC 103 (a) as being unpatentable over Chang et al. in view of Zheng et al (U.S. Patent No. 6,762,085). Claims 4, 8, 12, and 22-24 are rejected under 35 USC 103 (a) as being unpatentable over Chang et al. in view of Kasuya (U.S. Patent No. 6,784,078) and Zheng et al. Claims 25, 29, 33, 37, 38 and 40 are rejected under 35 USC 103 (a) as being unpatentable over Chang et al. in view of Jeng et al (U.S. Patent No. 6,136,643). Claims 26, 27, 30, 31, 34, 35, 39 and 40-48 are rejected under 35 USC 103 (a) as being unpatentable over Chang et al. in view of Jeng et al and Zheng et al. Claims 28, 32, 36 and 49-52 are rejected under 35 USC 103 (a) as being unpatentable over Chang et al. in view of Jeng et al, Kasuya, and Zheng et al.

As known in the art of nonvolatile memory (NVM), in general the memory device needs a layer or structure for charge injection into the trapping structure, as mentioned in the background or the references cited by the Applicant. Typically, the injection part is formed between the trapping structure and the substrate.

For example, in US Patent No. 4,881,108, figure 7 and corresponding description: "In the memory cell constituted above, when a high voltage, e.g., a voltage more than 20 volts is applied across the drain electrode 11 and the control gate 8, a tunnel current flows in a portion between the extending portion 6' of the floating gate 6 and the n.sup.+ type diffused region 4' via the insulating thin film 12. Thus, charge is injected into the floating gate 6 and is drained therefrom."

In the Specification, the applicant recites the following description in page 10, "Spacer 12 is used for charge trapping and is preferably comprised of silicon nitride. The hot electrons or holes are trapped as they are injected into the Spacer 12. The memory cell

is capable of storing two bits of data, a right bit and a left bit. The two bit memory cell is a symmetrical device."

Applicant has amended the rejected and objected matter noted by the Examiner. In view of the amendments above and the remarks set forth, Applicant respectfully requests reconsideration.

1. Rejection under 35 USC 102 (b) as being anticipated by Chang et al. (U. S. Patent No. 5,969,383).

Chang discloses a Split-gate memory device. Please refer to abstract of Chang... When programming the split gate FET (10), electrons are accelerated in a portion of a channel region (38) between the select gate (16) and the control gate (32), and then injected into a nitride layer (24) of an ONO stack (25) underlying the control gate (32). Please refer to page.4, lines 61~65 of Chang... Accessing NVM cell 10 of FIG. 1 includes three parts: programming NVM cell 10, erasing NVM cell 10, and reading data from NVM cell 10. These are achieved through biasing select gate 16, control gate 32, source region 36, and drain region 22 of NVM cell 10 to selected voltages. In other words, mechanism of accessing NVM cell 10 of Chang is utilized by controlling these two gates including select gate 16 and the control gate 32, respectively. In the Chang, a control gate 32 overlies ONO stack 25. Control gate 32 has a sidewall 31 adjacent select gate 16 and a sidewall 33 opposite to sidewall 31. Thus, the control gate of the citation is over the nitride layer of ONO. The unit cell of the memory is formed by the ONO 25 and the control gate 32. Thus, it only stores one bit in the ONO in one unit cell. It is impossible to store multiple bits.

Further, in Chang, a select gate structure 15 includes a dielectric layer 14 overlying substrate 11 and a select gate 16 over dielectric layer 14. Select gate 16 has sidewalls 17 and 18 opposite to each other. Please refer to the background of Chang, to program an EEPROM cell using source side hot carrier injection, a select gate is formed overlying a portion of the channel region adjacent the source region... The select gate controls the

channel current... Please refer to page 10, lines 11~14 of the present application...The control gate structure 6 corresponding to the similar location of gate 16 of Chang acts as the control gate not the select gate of Chang, and the nitride spacers of the present application are used to trap carriers. Thus, the control gate 6 of the present invention is over the gate dielectric on the substrate. The gate of Chang over the dielectric 14 over the substrate is the select gate 16. However, the control gate 32 of Chang is formed as the left-side spacer of the select gate 16. The location of the control gate is quite different.

In the present, the spacers 12 are used to store charges, thereby defining, for example, the digital states including (0, 0), (0, 1), (1, 0), (1, 1). Actually, the NVM cell of the present application uses the control gate 6 to access and storing carriers in the spacers 12. The spacers 12 are formed over the sidewall of the control gate. In the amendment claims, the first spacers include charge trapping capability thereby storing single or multiple bits of data. Chang fails to disclose or teach the first spacers 12 are formed over the sidewall of the control gate. However, please refer to the description and abstract of Chang, it mentioned that electrons are accelerated in a portion of a channel region (38) between the select gate (16) and the control gate (32), and then injected into a nitride layer (24) of an ONO stack (25) underlying the control gate (32). Apparently, the trapping nitride layer is formed underlying the control gate. It is apparently different from the claimed invention. Further, Chang fails to disclose or teach the usage of spacers for trapping carriers thereby storing two bits of data. Thus, Applicant believes that Chang does not anticipate the application under 35 USC 102 (b)

Moreover, Please refer to page.2, lines 50~51 of Chang..... A drain region 22 is aligned with sidewall 17 of select gate 16. Please refer to page.3, lines 60~61 of Chang..... A source region 36 is aligned with nitride spacer 34. The source region 36 is formed adjacent to the select-gate 16 under the nitride spacers 35 and the drain region 22 is formed adjacent to the nitride spacers 34. In other words, the drain region 22 and source region 36 of Chang are asymmetric. In contrast, the application discloses that the source and drain regions are symmetrically formed adjacent to but not aligned to the control gate

edge, and the drain regions and source regions of the application are symmetric. Both source and drain of the present application are not adjacent to the gate, and Chang's drain (#22) is adjacent to the select-gate edge (#16) and source(#36) is adjacent to control-gate(#32) edge. Chang fails to disclose that the source and drain regions are symmetrically formed adjacent to but not aligned to the control gate edge. Thus, Applicant believes that Chang does not anticipate the application under 35 USC 102 (b).

Furthermore, Please refer to page.3, lines 33~37 of Chang..... Control gate 32 has a sidewall 31 adjacent select gate 16 and a sidewall 33 opposite to sidewall 31. By way of example, control gate 32 is formed by depositing and patterning a conductive layer over ONO stack 25. Please refer to page.3, lines 57~60 of Chang..... Dielectric spacers such as, for example, nitride spacers 34 and 35 are formed along sidewall 33 of control gate 32 and along sidewall 17 of select gate 16, respectively. In other words, the spacers 32/34 and 35 of Chang are asymmetric and different in structures and materials (#32 is conductive layer and #34 & 35 are dielectric). In contrast, the application discloses that the first spacers are formed on the sidewall of the first isolation layer, that is, the drain regions and source regions of the application are symmetric. Chang fails to disclose that the first spacers are formed on the sidewall of the first isolation layer. Thus, Applicant believes that Chang does not anticipate the application under 35 USC 102 (b).

Claims 2-24, 26-52 are dependent claims of the amended claim 1, 25. In view of the foregoing remarks, Applicant respectfully request that the Examiner withdraw his rejections and the case be passed to issuance.

2. Rejection of Claims 2, 3, 6, 7, 10, 11 and 15-21 under 35 USC 103 (a) as being unpatentable over Chang et al.(U. S. Patent No. 5,969,383) in view of Zheng et al (U.S. Patent No. 6,762,085).

Zheng discloses a Method of forming a high performance and low cost CMOS device. Applicant would like to emphasize that the citation of Zheng is a CMOS transistor

that is used as a switch as well known in the art. However, the application is NVM (nonvolatile memory) that is read only memory. Where the prior art leads to an entirely different field, namely, not analogous art. NVM needs a charge storing or trapping layer or structure to store carriers or charge, MOS is a switch and therefore it does not perform such function, and therefore, no structure "for storing carrier" is needed. In normal MOS transistor operation mode, the spacer is used as isolation for the gate and to form LDD structure instead of storing charge. If charges are injected into the isolation spacer of MOS, the device will be fail. Thus, it is unlikely to combine Chang and Zheng.

Please refer to page .5, lines 29~36 of Zheng. The salicide blocking procedure and the formation of a composite spacer comprised of silicon nitride 14b, on thick silicon oxide component 4b, in NMOS region 30, and of a composite spacer comprised of silicon nitride layer 14a, on thick silicon oxide component 4b, in PMOS region 40, was accomplished using only a single photolithographic masking procedure. As know in the art, the spacer in the CMOS field is used to create doped region instead of forming trapping structure, therefore, there is no motivation for Zheng to form a spacer structure for trapping or storing carriers. Actually, Zheng does not exhibit the inherent function or intend to use it as an NVM because it is impossible for an MOS transistor to store carriers.

Moreover, there is no any suggestion or motivation of the combination of the citations indicates the limitations cited in the claims. It cannot found any motivation or suggestion from Chang and Zheng at the time of the invention filed to teach the claimed invention. The combination of Chang with Zheng fails to achieve the Claimed invention of the present invention as set in the Claims. Where the prior art leads to an entirely different field, namely, not analogous art. Pursuant to *Graham v. John Deere Co.*, 383 U. S. 1(1966), the obviousness rejection is overcome.

Applicant respectfully traverses the Examiner's rejection of 2, 3, 6, 7, 10, 11 and 15-21 under 35 USC 103 (a).

3. Rejection of Claims 4, 8, 12, and 22-24 under 35 USC 103 (a) as being un-patentable over Chang et al.(U. S. Patent No. 5,969,383) and further in view of Kasuya (U.S. Patent No. 6,784,078), and further in view of Zheng et al (U.S. Patent No. 6,762,085).

Kasuya disclosed methods for manufacturing semiconductor devices and semiconductor devices. Please refer to TECHNICAL FIELD of Kasuya. The present invention relates to semiconductor devices having a field effect transistor and methods for manufacturing the same, and more particularly, to semiconductor devices having a gate electrode that is formed from two or more layers and methods for manufacturing the same. Therefore, Kasuya also disclosed a transistor instead of the nonvolatile memory (NVM). As aforementioned, the prior art leads to an entirely different field, namely, not analogous art. The NVM needs a charge trapping structure to store carriers or charge, no structure "for storing carrier" is needed in MOS. Kasuya fails to teach the storing charge structure as NVMs.

Please refer to page 6, lines 66 ~ page 7 line 2 of Kasuya. The low concentration impurity diffusion layer 42 is formed in a manner to enclose the high concentration impurity diffusion layer 44, in other words, has a double drain structure (double diffused drain). Actually, double diffused drain structure of Kasuya constitutes the source and drain regions 40. In contrast, the double doped drain region of the present application is adjacent to the source and drain regions, wherein p-n junctions of the double doped drain regions is formed under the first spacers and the p-n junction of the double doped drain region is deeper than the one of the source and drain regions. In other others, the double drain structure of the present application has a specific function that must be claimed to differentiate from the Kasuya. Kasuya fails to disclose "double doped drain region adjacent to said source and drain regions, wherein p-n junctions of said double doped drain regions formed under said first spacers and the p-n junction of said double doped drain region is deeper than the one of said source and drain regions and said double doped drain region is closer to the channel under said gate structure than said source and drain regions and

the doping concentration of said double doped drain region is lower than the one of said source and drain regions”.

There is no any suggestion or motivation of the combination of the citations indicates the limitations cited in the claims. It cannot found any motivation or suggestion from Chang, Zheng and Kasuya at the time of the invention filed to teach the claimed invention. The combination of Chang, Zheng with Kasuya fails to achieve the Claimed invention. Where the prior art leads to an entirely different field, namely, not analogous art. The obviousness rejection is overcome.

Applicant respectfully traverses the Examiner's rejection of Claims 4, 8, 12, and 22-24 under 35 USC 103 (a).

4. Rejection of Claims 25, 29, 33, 37, 38 and 40 under 35 USC 103 (a) as being unpatentable over Chang et al.(U. S. Patent No. 5,969,383) in view of Jeng et al (U.S. Patent No. 6,136,643).

Jeng discloses a Method for fabricating capacitor-over-bit-line dynamic random access memory (DRAM) using self-aligned contact etching technology. Please refer to page.4, lines 61~65 of Jeng... For example, by forming N-well regions in a P-doped substrate, P-channel FETs can also be provided from which can be formed Complementary Metal-Oxide-Semiconductor (CMOS) circuits required for the peripheral circuits on the DRAM chip. Thus, DRAM chip of the Jeng includes a transistor. The NVM is totally different from the DRAM or MOS as will known in the art. Apparently, the prior art leads to an entirely different field, namely, not analogous art. NVM needs a long term charge storing structure to store carriers or charges; no injection portion and structure “for storing carriers” are needed in a MOS transistor. More important, Jeng fails to disclose the charge trapping structure as cited in the amended claims. In the present invention, the spacer structure has a specific function to trap charge for nonvolatile memory described in the claims.

It cannot found any motivation or suggestion from Chang and Jeng at the time of the invention filed to teach the claimed invention. The combination of Chang with Jeng fails to achieve the Claimed invention.

Applicant respectfully traverses the Examiner's rejection of Claims 25, 29, 33, 37, 38 and 40 under 35 USC 103 (a).

5. Rejection of Claims 26, 27, 30, 31, 34, 35, 39 and 40-48 under 35 USC 103 (a) as being un-patentable over Chang et al.(U. S. Patent No. 5,969,383) in view of Jeng et al (U.S. Patent No. 6,136,643) and further in view of Zheng et al (U.S. Patent No. 6,762,085).

As a mentioned above, the prior art leads to an entirely different field, namely, not analogous art. As said, NVM needs a long term charge storing structure. No structure "for storing carriers" and injection portion are needed in a MOS transistor. The combination can not achieve the claimed invention.

There is no any suggestion or motivation of the combination of the citations indicates the limitations cited in the claims. It cannot found any motivation or suggestion from Chang, Zheng and Jeng at the time of the invention filed to teach the claimed invention. The combination of Chang, Zheng with Jeng fails to achieve the Claimed invention. Where the prior art leads to an entirely different field, namely, not analogous art. The obviousness rejection is overcome.

Applicant respectfully traverses the Examiner's rejection of Claims 26, 27, 30, 31, 34, 35, 39 and 40-48 under 35 USC 103 (a).

6. Rejection of Claims 28, 32, 36 and 49-52 under 35 USC 103 (a) as being un-patentable over Chang et al.(U. S. Patent No. 5,969,383) in view of Jeng et al (U.S. Patent No. 6,136,643) and further in view of Kasuya (U.S. Patent No. 6,784,078) , and further in view of Zheng et al (U.S. Patent No. 6,762,085).

Similarly, as a mentioned above, the prior art leads to an entirely different field, namely, not analogous art. As said, NVM needs a long term charge storing structure. No structure "for storing carriers" and injection portion are needed in a MOS transistor. The combination can not achieve the claimed invention.

There is no any suggestion or motivation of the combination of the citations indicates the limitations cited in the claims. It cannot found any motivation or suggestion from Chang, Kasuya, Zheng and Jeng at the time of the invention filed to teach the claimed invention. The combination of Chang, Zheng, Kasuya with Jeng fails to achieve the Claimed invention. Where the prior art leads to an entirely different field, namely, not analogous art. The obviousness rejection is overcome.

Applicant respectfully traverses the Examiner's rejection of Claims 28, 32, 36 and 49-52 under 35 USC 103 (a).

Applicant has enclosed the required fee. However, if any additional fee is due, please charge our Deposit Account No. 50-0665, under Order No. 386998041US from which the undersigned is authorized to draw.

Dated:

7/19/08

Respectfully submitted,

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Attachments